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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,332	02/11/2004	Mihel Seitz	1115747-0002/2002P50543US	4916

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EXAMINER	
HUYNH, ANDY	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,332	SEITZ ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *18-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/11/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction Requirement dated 08/02/2005, Applicant has elected Invention of Species I (Claims **1-17**) is acknowledged. Accordingly, claims **31 and 32** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 02/11/2004. The references cited on the PTOL 1449 form have been considered.

Claim Objections

Claims **1 and 3-5** are objected to because of the following reasons.

In claim **1**, line 2, "the trench" should read –the trench region--, line 4, "trench region" should read –the trench region--, line 11, "the isolation collar" should read –the isolation collar region--, "the length of the transistor" should read –a length of the transistor--.

In claim **3**, line 1, "wherein the top portion ..." should read –wherein a top portion ...--.

In claims **4 and 5**, line 1, "the isolation collar" should read –the isolation collar region--, line 3, "about 50-1000" should read –about 50-100 nm--.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1, 2, 10, 12, 16 and 17** are rejected under 35 U.S.C. 102(b) as being anticipated by Mandelman et al. (USP 6,339,241 hereinafter referred to as "Mandelman").

Regarding claim **1**, Mandelman discloses in Figs. 1-5 and the corresponding texts as set forth in col. 4, line 65-col. 6, line 8, a vertical dynamic random access memory (DRAM) cell device fabricated within a trench region 24, 26 in a substrate 20, the trench having first and second opposing substantially vertical edges, the vertical DRAM cell comprising:

(a) a storage capacitor 32 formed within the trench region for storing electrical charge;

(b) a transistor 40 formed within the trench region above the storage capacitor;

(c) a buried strap 37 formed proximate to the first vertical edge between the storage capacitor and the transistor, the buried strap electrically coupling the storage capacitor and the transistor; and

(d) an isolation collar region 28 formed proximate to the second vertical edge of the trench, the isolation collar extending the length of the transistor.

Regarding claim **2**, Mandelman discloses in Figs. 1-5 the cell device further comprises a trench top oxide (TTO) region 36 comprising a bottom surface, the bottom surface located above

a top surface of the buried strap, wherein the trench top oxide and the buried strap are located between the transistor and the storage capacitor.

Regarding claims **10 and 12**, Mandelman discloses in Figs. 1-5 and the corresponding texts as set forth in col. 4, line 65-col. 6, line 8, a buried strap 37 for electrically connecting a transistor 40 and a storage capacitor 32 in a vertical dynamic random access memory (DRAM) cell device formed within a semiconductor substrate 20 and having a trench 24, 26 with first and second opposing vertical edges, the buried strap comprising: an electrically conducting region 40 formed within the trench, the electrically conducting region formed proximate to the first opposing edge between the transistor and storage capacitor, and laterally displaced from an isolation region/a shallow trench isolation (STI) region 7 formed on the second opposing vertical edge, the isolation region/the STI region extending from the semiconductor substrate surface along the second opposing vertical edge and terminating at an edge no lower than the electrically conducting region, the buried strap formed at or below edge of the isolation region/the STI region.

Regarding claims **16-17**, Mandelman discloses the electrically conducting region comprises doped/undoped polysilicon (col. 5, lines 39-42).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **3-9, 11, 13 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (USP 6,339,241 hereinafter referred to as "Mandelman").

Regarding claims **3-5, 7 and 9**, Mandelman discloses all the claimed limitations except for the top portion of the buried strap is vertically separated from the bottom surface of the trench top oxide by about 150 to 450 nm; the isolation collar has a bottom edge, the bottom edge extending below the vertical location of the buried strap top surface by about 50-100 nm; the one-sided strap has a vertical dimension in the range of about 30 to 150 nm, and a lateral dimension in the range of about 50-100 nm. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the top portion of the buried strap vertically separated from the bottom surface of the trench top oxide by about 150 to 450 nm; the isolation collar has a bottom edge, the bottom edge extending below the vertical location of the buried strap top surface by about 50-100 nm; the one-sided strap has a vertical dimension in the range of about 30 to 150 nm, and a lateral dimension in the range of about 50-100 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims **6 and 8**, Mandelman discloses in Fig. 5 the buried strap comprises a one-sided strap.

Regarding claims **11, 13 and 14**, Mandelman discloses all the claimed limitations except for the electrically conducting region formed proximate to the first opposing edge is laterally separated from the second opposing edge by about 50-110 nm; the shallow trench isolation

region has a depth no greater than about 250-350 nm; and the shallow trench isolation region has a depth no greater than about 50-150 nm. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the electrically conducting region formed proximate to the first opposing edge is laterally separated from the second opposing edge by about 50-110 nm; the shallow trench isolation region has a depth no greater than about 250-350 nm; and the shallow trench isolation region has a depth no greater than about 50-150 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claim **15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (USP 6,339,241 hereinafter referred to as "Mandelman") in view of Sommer et al. (US Pub. No.: 2005/0056873 A1 filed 12/23/2003 dated 03/17/2005 hereinafter referred to as "Sommer").

Mandelman discloses all the claimed limitations except for the shallow trench isolation region comprises an oxide collar for electrically isolating the transistor and the storage capacitor in the vertical DRAM cell device from potential cross talk with an adjacent DRAM cell device. Sommer teaches in Figs. 3B-4L that crosstalk between the buried-strap areas 18 of different memory cells M can be prevented by insulating trench pattern arranged below the level of the word lines WL both in first and in the second variant of the layout. For this purpose, insulating trenches can be arranged in horizontal and/or in vertical direction between the buried-strap areas (not shown here). Widening the word line isolation trenches STI into the semiconductor

substrate 1 in order to insulate the buried-strap areas from one another in the direction of the bit line of adjacent memory cells M is also conceivable as set forth in paragraph [0048]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of insulating trenches arranged in horizontal and/or in vertical direction between the buried-strap areas, as taught by Sommer to incorporate into and to modify the Mandelman's structure to arrive the claimed limitations in order to prevent crosstalk between the buried-strap areas of different memory cells.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

08/11/05

Andy Huynh

Patent Examiner